

1 CLAIMS:

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3 Having thus described our invention, what we claim as
4 new and desire to secure by Letters Patent is as
5 follows:

6

7 1. In an interconnection structure suitable for
8 flip-chip attachment of microelectronic device chips to
9 chip carriers, a three-layer ball limiting metallurgy
10 comprising:

11 an adhesion layer for deposition on a wafer or
12 substrate;

13 a solder reaction barrier layer of a material
14 selected from the group consisting of Ti, TiN, Ta,
15 TaN, Zr, ZrN, V and Ni; and

16 a solder wettable layer.

17

18 2. The interconnection structure of claim 1,
19 wherein the adhesion layer is formed of a material
20 selected from the group consisting of Cr, TiW, TiN,
21 TaN, Ti, Ta, Zr, and ZrN.

22

23 3. The interconnection structure of claim 1,
24 wherein the solder wettable layer is formed of a
25 material selected from the group consisting of Cu, Pd,
26 Co, Ni, Au, Pt, and Sn.

27

28 4. The interconnection structure of claim 1,
29 further comprising an optional fourth layer is formed

1 of a material selected from the group consisting of Au
2 and Sn, if Au or Sn is not used in the third layer.
3

4 5. The interconnection structure of claim 1, wherein
5 said adhesion layer is comprised of one of Cr and TiW,
6 said reaction barrier is comprised of Ti, and said
7 solder wettable layer is comprised of one of Cu, Co,
8 Ni, Pd and Pt.
9

10 6. An interconnection structure suitable for
11 flip-chip attachment of microelectronic device chips to
12 packages, comprising:

13 a two-layer ball-limiting composition comprising an
14 adhesion/reaction barrier layer, wherein the
15 adhesion/reaction barrier layer serves both as an
16 adhesion and reaction barrier layer, and a solder
17 wettable layer, said adhesion/barrier layer being for
18 placement between a microelectronic device and said
19 solder wettable layer, and wherein said solder wettable
20 layer is of a metal reactive with components of a
21 tin-containing lead-free solder, so that said solder
22 wettable layer is consumed during soldering, wherein
23 the adhesion/reaction barrier layer remains after being
24 placed in contact with said lead free solder during
25 soldering; and

26 one or more lead-free solder balls selectively
27 situated on said solder wettable layer, said lead-free
28 solder balls comprising tin as a predominant component
29 and one or more alloying components.
30

1 7. The interconnection structure defined in claim 6,
2 wherein said adhesion/reaction barrier layer is
3 comprised of a material selected from the group
4 consisting of Ti, TiN, TiW, Ta, TaN, Zr, ZrN and V.

5
6 8. The interconnection structure defined in claim 6,
7 wherein said solder wetting layer is comprised of a
8 material selected from the group consisting of Cu, Ni,
9 Co, Pd, Pt, Au and Sn.

10
11 9. The interconnection structure defined in claim 6,
12 further comprising an optional third layer comprised of
13 Au or Sn, if the second layer is not formed of Au or
14 Sn.

15
16 10. The interconnection structure defined in claim
17 6, wherein said lead-free solder ball is comprised of a
18 material that substantially avoids alpha particle
19 emission.

20
21 11. The interconnection structure defined in claim
22 6, wherein said alloying components are selected from
23 the group consisting of Sn, Bi, Cu, Ag, Zn and Sb.

24
25 12. The interconnection structure defined in claim
26 6, adhesion/reaction barrier layer comprises Ti and
27 said solderable layer comprises one of Cu, Co, Ni, Pd
28 and Pt.

1 13. An interconnection structure suitable for
2 flip-chip attachment of microelectronic device chips to
3 packages, comprising:

4
5 a three-layer ball-limiting composition comprising
6 an adhesion layer, a reaction barrier layer on top of
7 said adhesion layer and a solder wettable layer,
8 wherein said adhesion/barrier layer is between a
9 microelectronic device and said solder wettable layer
10 and wherein said solder wettable layer is of a
11 composition sufficiently reactive with components of a
12 tin-containing lead free solder, and the reaction
13 barrier layer is substantially less-reactive with
14 solder after being placed in contact therewith in a
15 solder joining process; and

16
17 one or more lead-free solder balls selectively
18 situated on said solder wettable layer, said lead-free
19 solder balls having tin as a predominant component and
20 one or more alloying components selected from the group
21 consisting of Cu, Zn, Ag, Bi and Sb, whereby said
22 lead-free solder ball substantially avoids alpha
23 particle emission and induced soft logic errors which
24 result therefrom.

25
26 14. The interconnection structure defined in claim
27 13, wherein said solderable layer is formed of a
28 material selected from the group consisting of Cu, Ni,
29 Co, Pd, PdNi, PdCo, NiCo, Au, Pt and Sn.

1 15. A method for forming an interconnection
2 structure suitable for flip-chip attachment of
3 microelectronic device chips to packages, comprising:

4 forming a ball limiting composition on a
5 substrate;

6 forming a resist pattern on the ball limiting
7 composition;

8 etching the ball limiting composition by using the
9 resist as an etch mask;

10 removing the resist from remaining ball limiting
11 composition; and

12 depositing solder on the ball limiting
13 composition.

14
15 16. A method as recited in claim 15, wherein the
16 solder is substantially lead free.

17
18 17. A method as recited in claim 15, wherein the
19 ball limiting composition is formed by:

20 depositing an adhesion layer on said substrate;

21 depositing a reaction barrier layer on said
22 adhesion layer; and

23 depositing a solder wettable layer on said barrier
24 layer.

25
26 18. A method as recited in claim 17, wherein said
27 reaction barrier layer is comprised of a material
28 selected from the group consisting of Ti, TiN, Ta,
29 TaN, Zr, ZnN, V and Ni.

30

1 19. A method as recited in claim 17, wherein said
2 adhesion layer is deposited by sputtering, plating or
3 evaporating.

4
5 20. A method as recited in claim 17, wherein said
6 adhesion layer is deposited so as to have a thickness
7 of about 100 to about 4000 Angstroms.

8
9 21. A method as recited in claim 17, wherein said
10 reaction barrier layer is deposited by sputtering,
11 plating or evaporation.

12
13 22. A method as recited in claim 21, wherein said
14 reaction barrier layer is deposited so as to have a
15 thickness of about 100 to about 20,000 angstroms.

16
17 23. A method as recited in claim 17, wherein said
18 solder wettable layer is deposited by sputtering,
19 plating or evaporation.

20
21 24. A method as recited in claim 17, wherein said
22 solder wettable layer is deposited so as to have a
23 thickness of about 100 to about 20,000 angstroms.

24
25 25. A method as recited in claim 17, further
26 comprising depositing a layer comprising Au or Sn on
27 said solder wettable layer.

28
29 26. A method as recited in claim 25, wherein the
30 layer deposited on said solder wettable layer has a

1 thickness of between substantially 100 to substantially
2 20,000 angstroms.

3

4 27. A method as recited in claim 25, wherein the
5 layer deposited on said solder wettable layer is
6 deposited by one of sputtering, electro- or electroless
7 plating or evaporation.

8

9 28. A method as recited in claim 15, wherein the
10 ball limiting composition is formed by:

11 depositing an adhesion/reaction barrier layer on
12 said substrate; and

13 depositing a solder wettable layer on said barrier
14 layer.

15

16 29. A method as recited in claim 15, further
17 comprising annealing the ball limiting composition at
18 150 - 250 degrees C for 30 to 60 minutes.

19

20 30. A method for forming an interconnection
21 structure suitable for flip-chip attachment of
22 microelectronic device chips to chip carriers,
23 comprising:

24 depositing an adhesion layer on a wafer or
25 substrate serving as said chip carrier;

26 depositing a solder reaction barrier layer on said
27 adhesion layer;

28 depositing a solder wettable layer on said
29 reaction barrier layer;

1 depositing a lead free solder on said solder
2 wettable layer; and

3 reflowing said solder so that said solder wettable
4 layer diffuses into said lead free solder.

5

6 31. A method as recited in claim 30, wherein said
7 solder wettable layer contains Cu, and said Cu diffuses
8 into said solder.

9

10 32. A method as recited in claim 31, wherein said
11 lead free solder is substantially pure Sn, and a binary
12 Sn-Cu lead-free solder is formed during reflowing.

13

14 33. A method as recited in claim 31, wherein said
15 lead free solder is substantially binary Sn-Ag, and a
16 ternary Sn-Ag-Cu lead-free solder is formed during
17 reflowing.

18

19 34. A method as recited in claim 33, wherein a
20 eutectic solder is formed.

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22 35. A method as recited in claim 30, wherein a
23 number of elements in said solder is increased by at
24 least one element, by said diffusion.

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26 36. A method as recited in claim 30, further
27 comprising annealing at 150 - 250 degrees C for 30 to
28 60 minutes.

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1 37. A method for forming an interconnection
2 structure suitable for flip=chip attachment of
3 microelectronic device chips to chip carriers,
4 comprising:

5 depositing an adhesion layer on a wafer or
6 substrate serving as said chip carrier;

7 depositing a solder reaction barrier layer which
8 is solder wettable on said adhesion layer;

9 depositing a lead free solder on said solder
10 wettable layer; and

11 reflowing said solder so that said solder wettable
12 layer diffuses into said lead free solder.

13
14 38. A method as recited in claim 37, wherein said
15 solder wettable layer contains Cu, and said Cu
16 dissolves into said solder.

17
18 39. A method as recited in claim 38, wherein said
19 lead free solder is substantially pure Sn, and a binary
20 Sn-Cu lead-free solder is formed during reflowing.

21
22 40. A method as recited in claim 38, wherein said
23 lead free solder is substantially pure Sn-Ag, and a
24 ternary Sn-Ag-Cu lead-free solder is formed during
25 reflowing.

26
27 41. A method as recited in claim 40, wherein a
28 eutectic solder is formed.

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1 42. A method as recited in claim 37, wherein a
2 number of elements in said solder is increased by at
3 least one element, by said Cu dissolution.
4

5 43. A method as recited in claim 37, further
6 comprising annealing at 150 - 250 degrees C for 30 to
7 60 minutes.
8

9 44. A three layer ball limiting structure
10 comprising a Cr adhesion layer for placement on a
11 substrate; a Cu seed layer and a Ni reaction barrier
12 layer on the Cu layer.
13

14 45. The structure defined in claim 44, further
15 comprising a lead free solder composition in which the
16 Ni layer is reacted with solder during reflow of the
17 solder.
18

19 46. A four layer structure comprising a Cr
20 adhesion layer for deposit on a substrate, a Cu layer
21 on the Cr layer, a Ni reaction barrier layer on said Cu
22 layer, a layer of Cu on top of the Ni layer, said layer
23 of Cu being for dissolving into a lead-free solder to
24 form a binary Sn-Cu alloy or a ternary Sn-Ag-Cu alloy
25 from a plated pure Sn or binary Sn-Ag solder,
26 respectively.